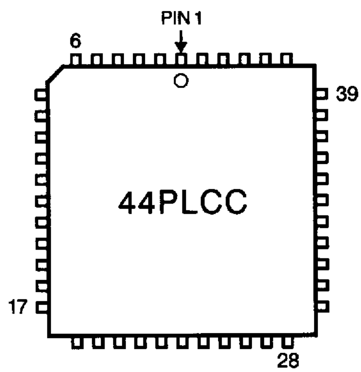
iFX730
10 ns FLEXlogic FPGA FAMILY WITH SRAM OPTION

- **High Performance FPGA (Field Programmable Gate Array)**
  - **Deterministic 10 ns Pin-to-Pin Propagation Delays**
  - **80 MHz System Clock Frequency**
- **Up to 30 Complex Macrocells**
  - **1,300 Equivalent Logic Gates or up to 3,840 Bits of SRAM**
- **0.8μ CMOS Technology**
  - **Power Management Options Minimize Active Power Consumption (1 mA/MHz)**
  - **1 mA Standby Version Available**
- **JTAG 1149.1 Compatible Test Port**
  - **Supports Boundary Scan and In-Circuit Reconfiguration/Programming**
- **Three Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix**
  - **Improves Fitting of Complex Designs**
- **Any CFB Can Be Either 24V10 Logic or SRAM Block**
  - **128 x 10 SRAM Configuration**
  - **CFB Selectable 3.3V or 5V Outputs**
  - **Open-Drain Output Option**
- **24V10 Macrocell Features**
  - **Dual Feedback on All I/O Pins**
  - **Allocation Supports up to 16 Product Terms per Macrocell with No Performance Penalty**
  - **12 Clocking Options**
  - **Flexible Preset/Clear Options**
  - **Selectable D/T Flip-Flops**
  - **Fast 12-Bit Identity Compare Option**
- **Supported by Industry Standard Design and Programming Tools**



290527-1

Package Options

Pins	Package	Macrocells	I/O	Inputs	Clocks	JTAG/V_{PP}	V_{CC}	GND
44	PLCC	30	25	5	2	5	3	4

April 1994 Order Number: 290527-001

INTRODUCTION

The iFX730 is a member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX730 consists of three configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 1300 gates of logic in a PLCC package.

FLEXIBLE PERFORMANCE

The iFX730 uses Intel's 0.8μ CHMOS EPROM technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

FLEXIBLE FEATURES

The unique combination of features available in the iFX730 makes it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX730 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

FLEXIBLE TESTING AND PROGRAMMING

The iFX730 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration, and programming modes. In-circuit reconfiguration not only allows the designer ultimate flexibility in prototyping new designs but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX730 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time.

FLEXIBLE TOOLS SUPPORT

The FLEXlogic FPGA family is supported by industry standard design entry and programming environments including Intel's PLDshell Plus software. This software runs on Intel386™ or higher PC-compatible platforms.

INTERCONNECT

The Global interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

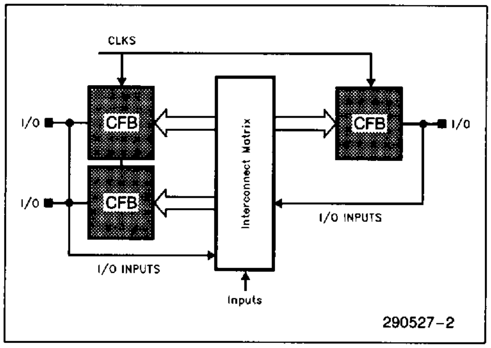


Figure 1. Interconnect Matrix

CONFIGURABLE FUNCTION BLOCKS

24V10 Mode

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a generous fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX730 architecture by providing more available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

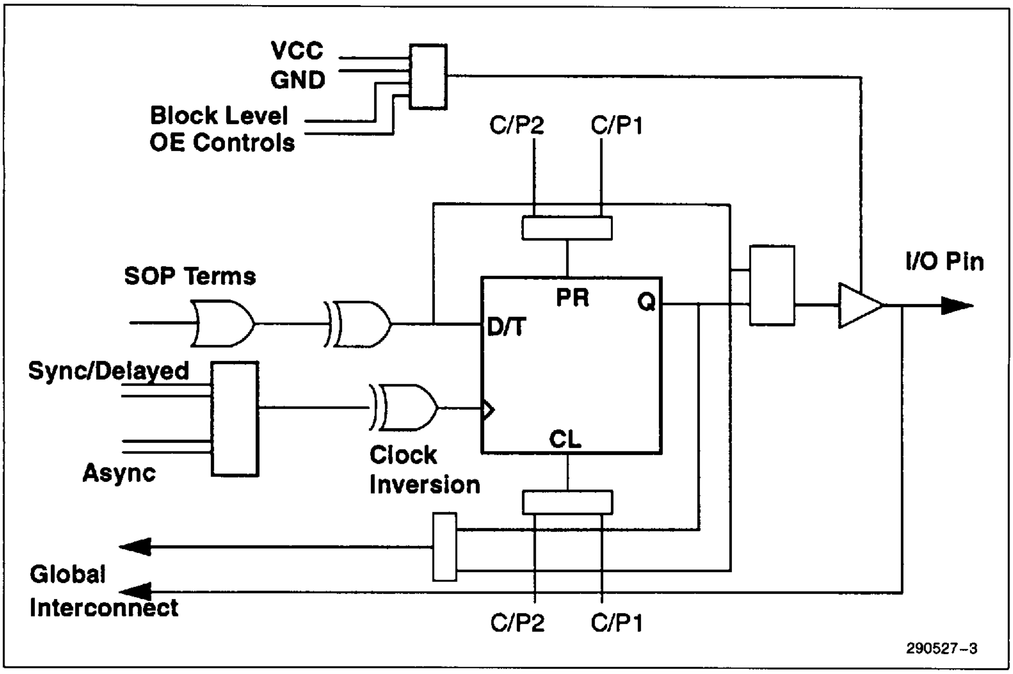


Figure 2. CFB as 24V10 Block

MACROCELL CONFIGURATIONS

Each I/O of the device has dual (internal and pin) feedback paths (see Figure 2). This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available as software emulations.

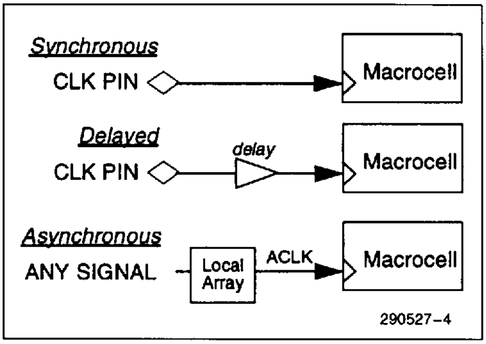


Figure 3. Clock Modes

CLOCKING MODES

There are three clocking modes available for every macrocell (see Figure 3): *synchronous*, *delayed*, *asynchronous*. Table 1 shows the different timing options each clock mode offers.

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Clock Mode Timings for iFX730

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6	0	6.5
Delayed	4.5	2	8.5
Asynchronous	1.5	5	12.5

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

CONTROL SIGNALS

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

COMPARATOR LOGIC

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals within the TPD of the device.

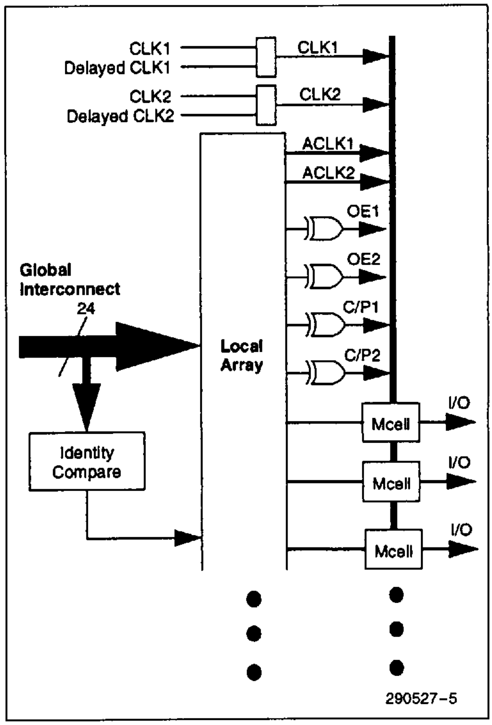


Figure 4. Control Signals

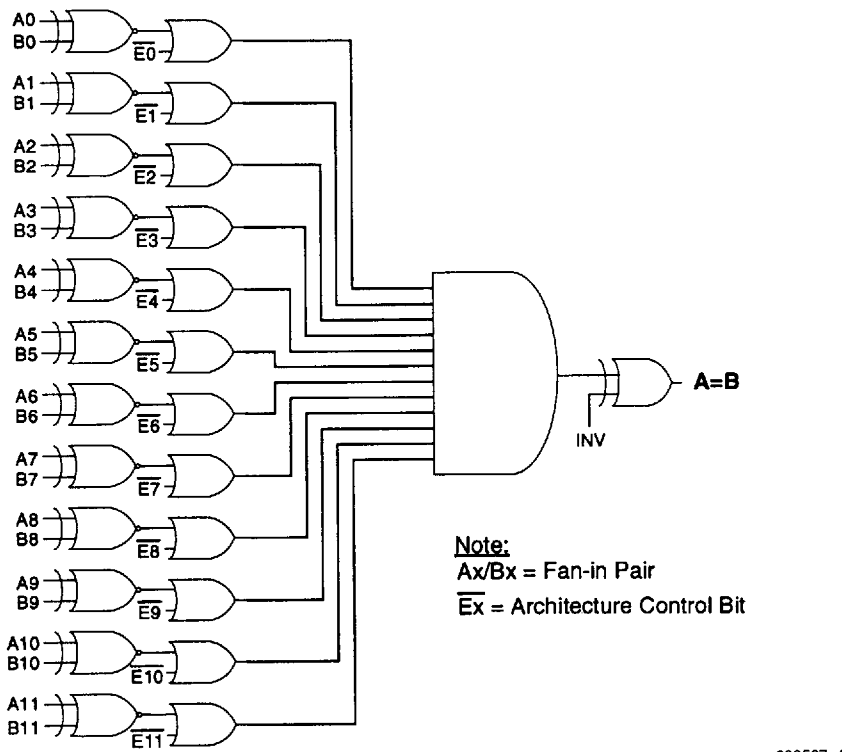


Figure 5. 12-Bit Identity Compare Logic

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24 − 16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

PRODUCT TERM ALLOCATION

The iFX730 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 or 16 P-terms are being used.

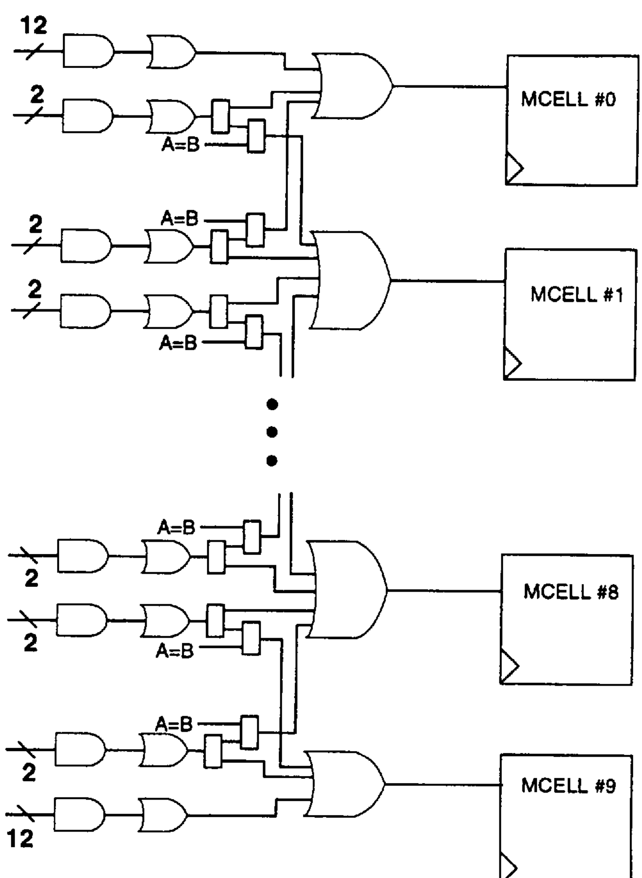


Figure 6. CFB Product Terms

SRAM Configuration

Each iFX730 CFB block can be configured as a 128 x 10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for $\overline{BE}$ (Block Enable), $\overline{WE}$, and $\overline{OE}$ controls (see Table 1).

Table 1. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$	$\overline{WE}$	$\overline{OE}$		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip non-volatile configuration cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and p-terms have been converted to SRAM use.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs, the "CMOS_LEVEL" keyword (the default condition for PLDasm) should be used. For TTL or 3.3V CMOS inputs, the "TTL_LEVEL" keyword should be used to minimize standby power consumption. Third party tools that support the FLEXlogic family provide input configuration in a method specific to each tool. For Additional information refer to Application Brief AB-27.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the iFX730 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX730 to be used in mixed voltage systems. For example, the iFX730 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

OPEN DRAIN OUTPUT OPTION

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL VERSUS CMOS OUTPUTS

There is a weak pullup provided for CMOS-compatible outputs. This pullup is always active in both 3.3V and 5V modes.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX730. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX730 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX730 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one de-

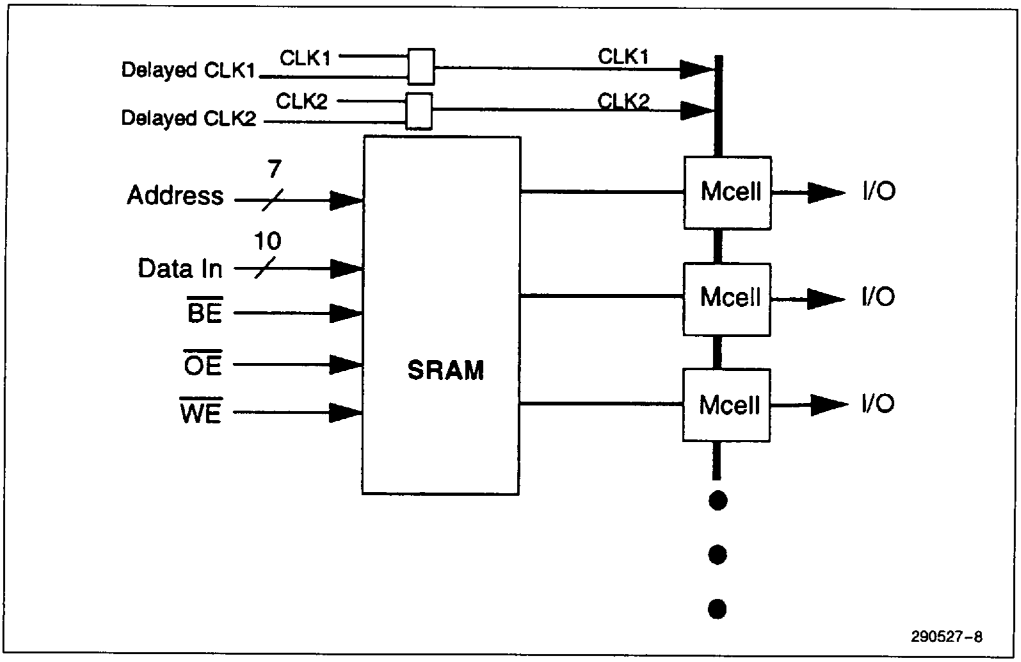


Figure 7. SRAM Overall Block Diagram

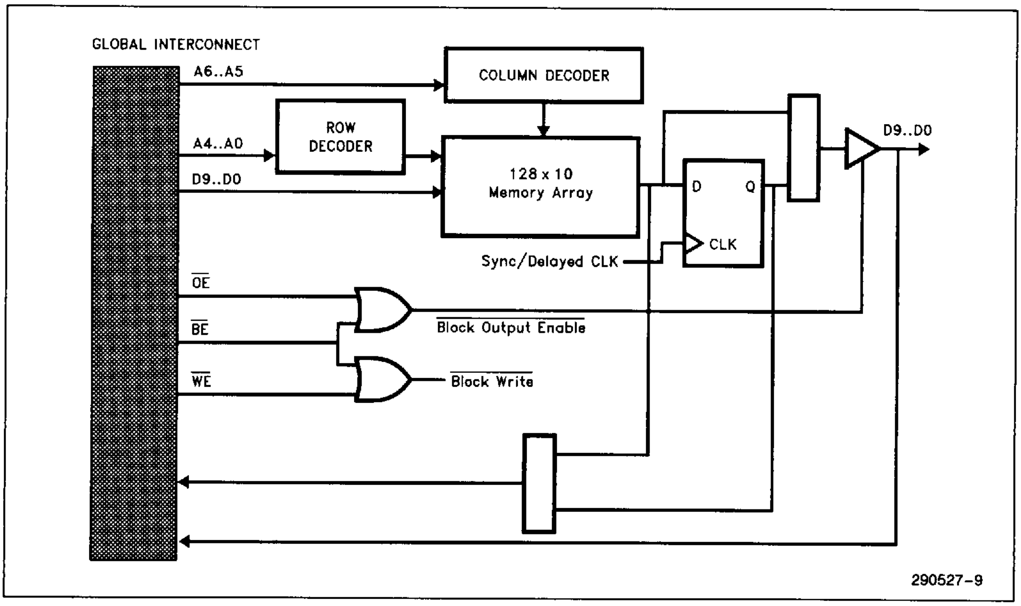


Figure 8. SRAM Functional Block Diagram

4826176 0086753 328

vice while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX730 for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX730 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR opcode 00000 binary):

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX730 package, typically for printed circuit board interconnects.

BYPASS (IR opcode 11111 binary):

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR opcode 00001 binary):

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snapshot of the values of the pins of the iFX730 in an unobtrusive manner and 2) preloads data to the iFX730 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR opcode 00010 binary):

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the IDcode to be serially shifted out of TDO.

UESCODE (IR opcode 10110 binary):

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR opcode 01000 binary):

The HIZ instruction sets all I/Os to a high impedance state.

IN-CIRCUIT RECONFIGURATION

The iFX730 supports in-circuit reconfiguration and in-circuit programming through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device.

This may be done as many times as desired in a prototyping scenario. Once the final version of the design is confirmed it may be programmed into the non-volatile cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pin (V_{PP}).

For more details on in-circuit reconfiguration and programming please refer to the iFX730 Device Programming and In-Circuit Reconfiguration Specification and supporting application notes.

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the non-volatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

— Design Merge
— SRAM Configuration Support
— Compare Operation Support
— Simulation Support for Intel FPGA
— Vector Notation
— Full Mouse Support
— Device Selector

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX730. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA ARCHITECTURAL FEATURE SUPPORT

PLDshell Plus supports all of the innovative architectural features of the iFX730 through the implementation of new language syntax such as:

- SRAM configuration
- Compare operation
- Buried macrocells
- Clocking options
- 3.3V and 5V options

FUNCTIONAL SIMULATION

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

- Event-driven simulation of combinatorial, registered, and state machine designs
- Ability to set any input, preload any register, and compare any output against an expected value
- Ability to group signals together (form a vector) to simulate a bus
- Generation of test vectors from simulation results for inclusion in the JEDEC file
- Simulation history file with ability to output a subset of signals to a secondary trace file

DEVICE SELECTOR

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

SYSTEM REQUIREMENTS

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

- Intel 386 based PC compatible
- 4MB RAM (minimum)
- VGA monitor/adaptor
- DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

The Intel FLEXlogic family of FPGAs and the iPLD line of devices are supported by industry leading third-party design tools. Support on the most popular low-end and high-end third party design tools is offered by Intel by combining the powerful Intel FLEXlogic Fitter into all of its third-party offerings: Intel Fitter Kits for design tools, FLEXlogic Plus Design Kits for CAE tools, and Intel's PRO iDesign—an OEM Design Tool partnering with Viewlogic.

Intel Fitter Kits

- **Data I/O**
  - ABEL—Design software offering four design entry methods to describe and implement logic designs, plus functional simulation.
- **Logical Devices**
  - CUPL Total Design—A high-level, universal design software package with many design expression formats and simulation support.
- **MINC**
  - PLDesigner-XL—A powerful design tool offering MINC's unique optimization, design partitioning, functional simulation and integration with your other EDA tools.
- **OrCAD**
  - OrCAD PLD—Integrates OrCAD's powerful schematic entry, compile and simulation tools for a complete PLD and FPGA design solution.

Intel FLEXlogic Plus Design Kits

Support on leading third-party CAE tools is provided by Intel's FLEXlogic Plus Design Kits, which run under Viewlogic's Workview and Powerview design software. Existing Workview and Powerview users continue to use the familiar features of Viewlogic's CAE design software with the addition of the powerful FLEXlogic Fitter which uses Intel's Adaptive Fitter Technology (AFT). Developed along in tandem with new devices, AFT utilizes an incremental algorithm offering 95% resource utilization over 95% of the time.

Intel PRO iDesign Series Software

PRO iDesign partners Viewlogic's PROcapture, PROsim and PROwave with Intel's powerful FLEXlogic fitter and Adaptive Fitter Technology (AFT). PRO iDesign is a PRO Series, Windows-based CAE software package licensed by Viewlogic. This integrated design tool sold by Intel is an affordable design entry path to all Intel FLEXlogic FPGAs and iPLD devices.

Additional Support

Support on two other popular design tools is offered by Intel by combining the Intel FLEXlogic Fitter into the Mentor PLDsynthesis 2 fitting tool containing the MINC fitter and into the MINC PLDesigner-XL product for Synopsys.

- **Mentor Falcon Frameworks**—Supports Intel's FPGAs and PLDs by adding mentor's PLDsynthesis 2 synthesis and fitting tool with a seamless user interface to Mentor's Design Architect and Autologic. The PLDsynthesis 2 product bundles the Intel FLEXlogic Fitter into its PLDesigner-XL software to provide support in the Mentor environment for all FLEXlogic FPGAs and iPLDs in all package types.
- **Synopsys**—Offers industry-leading VHDL and Verilog HDL synthesis and compilation capabilities in designing with FLEXlogic FPGAs and the iPLD line of devices. This is accomplished by the seamless integration of MINC's PLDesigner-XL design tool with the FLEXlogic Fitter. Engineers get the behavioral design entry of the Synopsys Design Compiler, with the language interface, device selection, and place-and-route capabilities of MINC's PLDesigner-XL, and the Adaptive Fitter Technology of Intel's FLEXlogic Fitter.

PROGRAMMING SUPPORT

Programming Support will be provided by a number of leading vendors, such as:

- Products in Motion (916) 363-0571
  - PROTAG JTAG Programmer
- BP Microsystems
  - PLD 1100
- Data I/O
  - Unisite
  - 2900/3900
- Elan
  - Model 6000
- Advin Systems Inc
  - PILOT-U84
  - PILOT-U40
- Logical Devices
  - ALLPRO
- SMS
  - Sprint Plus

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
  - Smart Model: Device model support for behavioral simulation through a variety of simulators.

ORDERING INFORMATION

f_{CNT1} (MHz)	F_{MAX} (MHz)	t_{PD} (ns)	I_{SB} (mA)	I_{CC} (mA/MHz)	Order Code	Package
80	100	10	20	1.0	N44FX730-10	44-Pin PLCC
50	66.7	15	20	1.0	N44FX730-12	44-Pin PLCC

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

DC Input Voltage (V_I)(1, 2) .... −0.5V to V_{CC} +0.5V

Storage Temperature (t_{stg}) ...... −65°C to +150°C

Ambient Temperature (t_{amb})(3) ... −10°C to +85°C

NOTES:

1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage −5V	4.75	5.25	V
V_{CCO}	Output Supply Voltage −3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4)

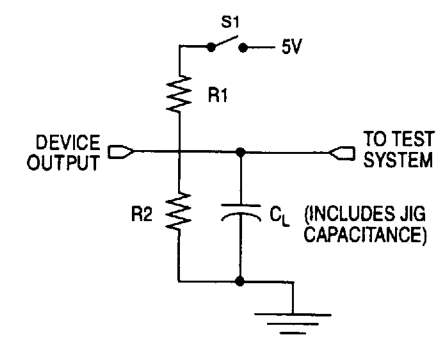
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(5)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	5V TTL High Level Output	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min.
	5V CMOS High Level Output	V_{CC} −0.2			V	I/O = −20 µA D.C., V_{CC} = Min.
	3V High Level Output Voltage	V_{CC} −0.2			V	I/O = −20 µA D.C., V_{CC} = Min.
V_{OL}	5V Low Level Output Voltage			0.45	V	I/O = 12 mA D.C., V_{CC} = Min.
	3V Low Level Output Voltage			0.2	V	I/O = 20 µA D.C., V_{CC} = Min.
I_I(10)	Input Leakage Current			±10	µA	V_{CC} = Max., V_{IN} = GND or V_{CC}
I_{OZ}	Output Leakage Current			±50	µA	V_{CC} = Max., V_{OUT} = GND or V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{SB}	Standby Power Supply Current iFX730		20		mA	$V_{IN} = V_{CC}$ or GND, Outputs Open
I_{CC} Active	Power Supply Current iFX730		1		mA per MHz	$V_{IN} = V_{CC}$ or GND, Device Programmed a Two 15-Bit Counters

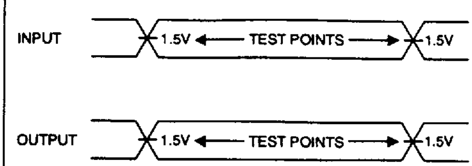
NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
10. Input leakage current on JTAG pins: ±25 μA.

A.C. TESTING LOAD CIRCUIT



290527-10

A.C. TESTING INPUT, OUTPUT WAVEFORM



290527-11

NOTE:
Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times <3 ns.

SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial		Measured Output Value
			R1	R2	
t_{PD}	Closed	35 pF	330Ω	200Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: $V_{OH} - 0.5V$ L → Z: $V_{OL} + 0.5V$

PIN CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz		10	12	pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz		12	15	pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz		15	18	pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz		12	15	pF

NOTES:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10			-12			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or I/O to Output Valid			10			12	ns
t_{PZX}(8)	Input or I/O to Output Enable			12			15	ns
t_{PXZ}(8)	Input or I/O to Output Disable			12			15	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			18	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			12	ns

REGISTER MODE—iFX730-10 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$ - External Feedback	80		76.9		71.4		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$ - Internal Feedback	80		76.9		71.4		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$ - No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6		4.5		1.5		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6.5		8.5		12.5	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16.5		18.5		22.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4.5		4.5		5		ns
t_{CH}	CLK High Time	4.5		4.5		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

NOTE:

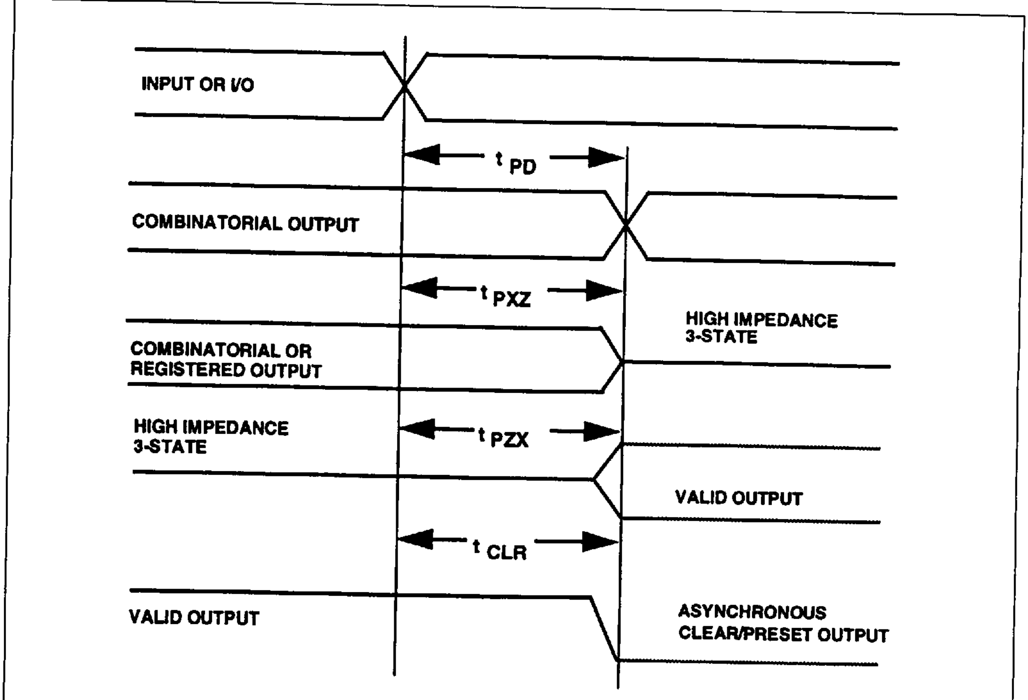
8. T_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measured with A C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

REGISTER MODE—iFX730-12 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

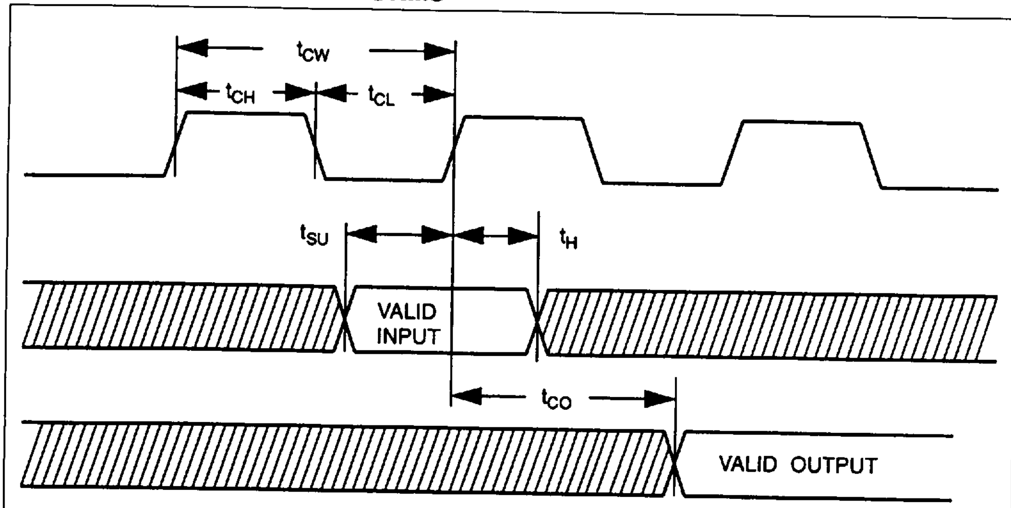
Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$ - External Feedback	66		62.5		58.8		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$ - Internal Feedback	66		62.5		58.8		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$ - No Feedback	80		74		64		MHz
t_{SU}	Input or I/O Setup Time to CLK	7.5		6		2.5		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		7.5		10		14.5	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		19.5		22		26.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		15		16		17	ns
t_{CL}	CLK Low Time	5		5		6		ns
t_{CH}	CLK High Time	5		5		6		ns
t_{CP}	CLK Period	12.5		12.5		15		ns

COMBINATORIAL MODE WAVEFORMS



290527-12

REGISTERED MODE WAVEFORMS

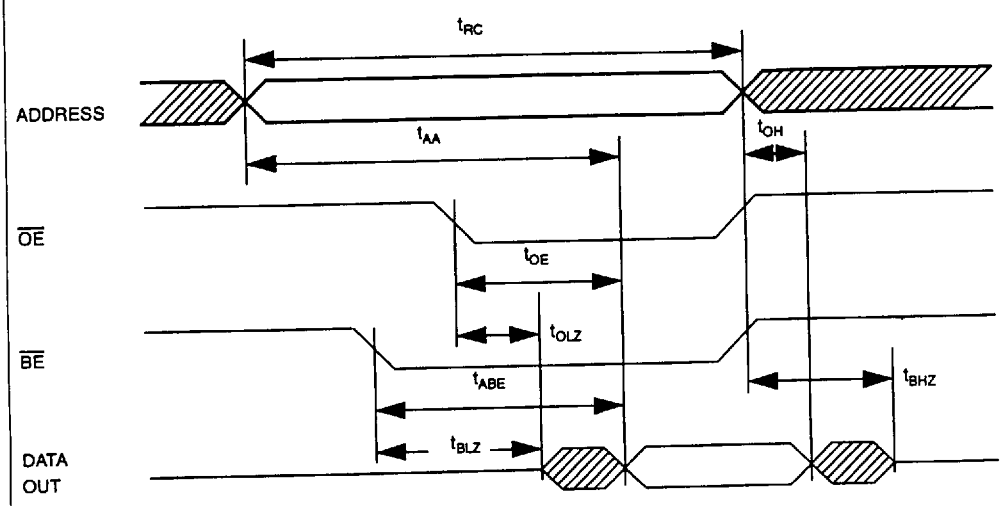


290527-13

SRAM READ—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10		-12		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address Access Time		15		20	ns
t_{ABE}	Block Enable Access Time		15		20	ns
t_{OE}(1)	Output Enable to Output Valid		12		15	ns
t_{OH}	Output Hold from Address Change	2		3		ns
t_{BLZ}(1)	Block Enable to Output in Low Z	3		5		ns
t_{BHZ}(1, 2)	Block Disable to Output in High Z		12		15	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	3		5		ns

TIMING WAVEFORM OF READ CYCLE



Note: $\overline{WE}$ held at V_{IH}

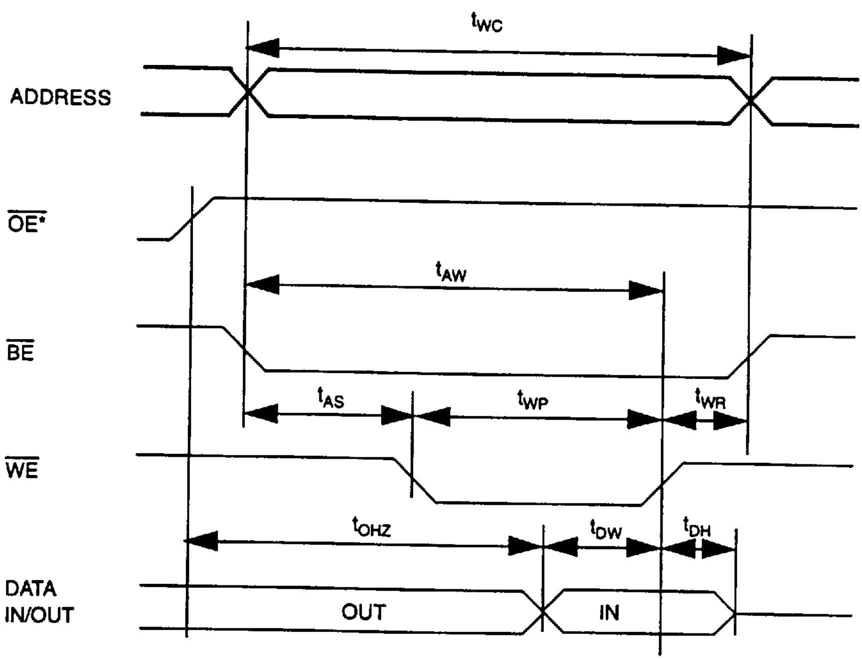
290527-14

SRAM WRITE—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	-10		-12		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		ns
t_{BW}	Block Enable to End of Write	10		13		ns
t_{AW}	Address Valid to End of Write	13		17		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	10		13		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		13		ns
t_{DH}	Data Hold Time	2		3		ns
t_{OHZ}(1, 2, 3)	Output Disable to Valid Data In	12		15		ns

NOTES:
1. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5V on output.
2. These signals are measured with C_L = 5 pF.
3. Does not apply for separate data in and data out buses.

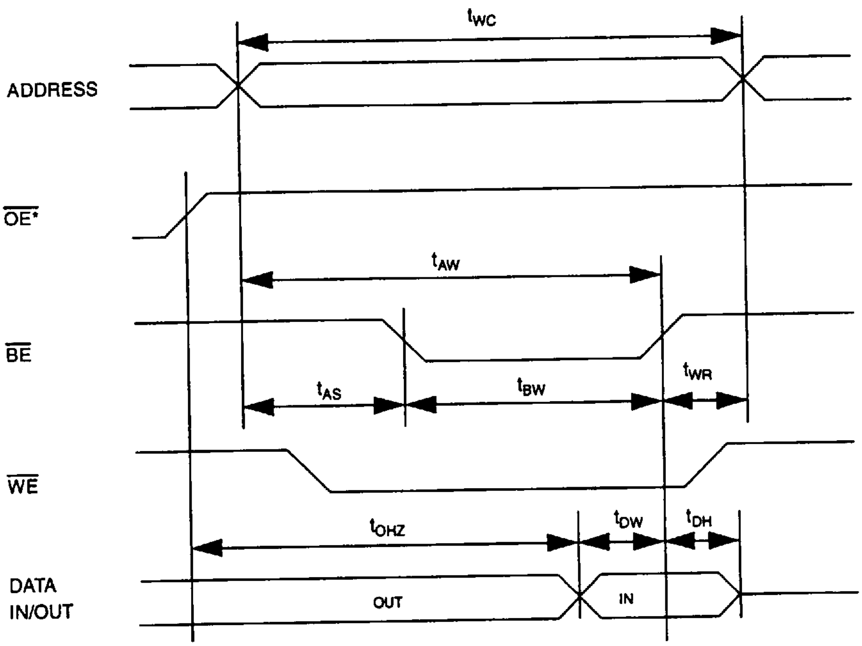
TIMING WAVEFORM OF WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED TIMING)



*Note: Cycle shown is for common data in and data out bus.

290527-15

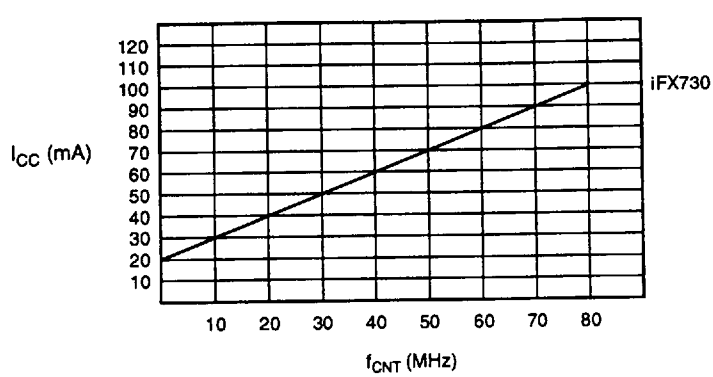
TIMING WAVEFORM OF WRITE CYCLE #2 ($\overline{BE}$ CONTROLLED TIMING)



*Note: Cycle shown is for common data in and data out bus.

290527-16

I_{CC} vs FREQUENCY



Conditions: TA = +25°C, VCC = 5V

(Note: Two 15-bit counters)

290527-17

POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, the power-up cycle time varies. For a monotonic V_{CC} rise (1 ms/V min.), the power-up cycle is complete when V_{CC} reaches the V_{CC} min. value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. During power-up I/Os are held high by an active weak pullup. The outputs on an unprogrammed device are placed in a high impedance state upon completion of power-up cycle.

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

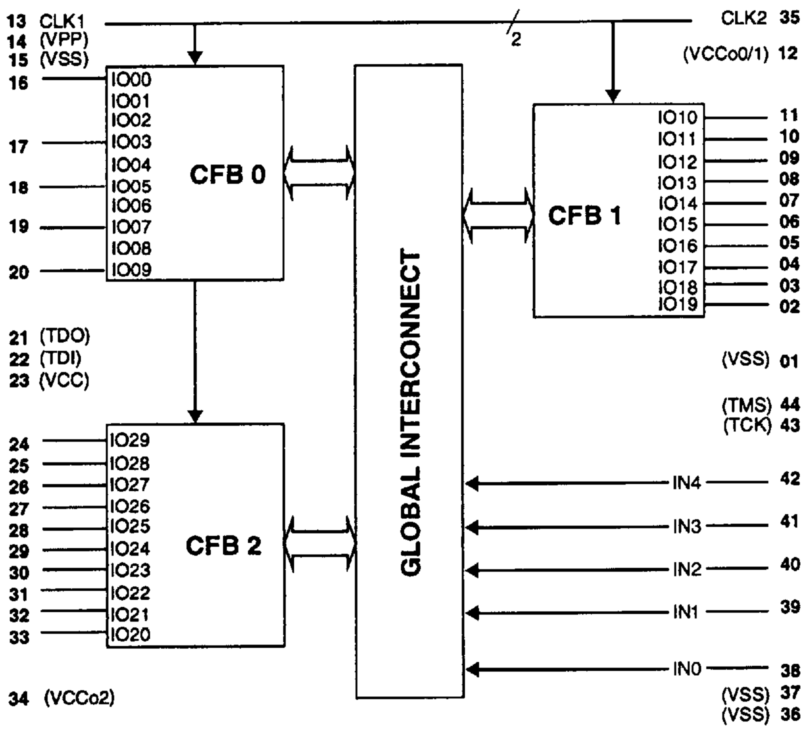
Pin Name	Description
V_{CC}	Supply voltage for the iFX730. All must be connected to 5V.
V_{SS}	Ground connections for the iFX730. All must be connected to GND.
V_{PP}	Programming voltage for the iFX730. During programming, 12.75V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC}, V_{PP} or left floating (not GND).
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V_{CC} or GND.
TDI	The Testability Data input is the boundary scan serial data input to the iFX730. JTAG instructions and data are shifted into the iFX730 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX730. JTAG instructions and data are shifted out of the iFX730 on the TDO output on the failing edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the iFX730. TCK is used to clock state information and data into and out of the iFX730 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the iFX730. TMS may be left floating if unused.

Table 5 lists the user-defined pin names and descriptions.

Table 5. User-defined Pins

Pin Name	Description
V_{CCOx}	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to the desired output drive voltage.
CLKx	Global clocks.
I/Oxx	Pins that can be configured either as an input or an output. Unused I/O pins should be connected to V_{CC} or GND.

44-PIN PLCC PACKAGE



290527-18

intel®

NORTH AMERICAN SALES OFFICES

ALABAMA

Intel Corp.
600 Boulevard South
Suite 104-I
Huntsville 35802
Tel: (800) 628-8686
FAX: (205) 883-3511

ARIZONA

†Intel Corp.
410 North 44th Street
Suite 500
Phoenix 85008
Tel: (800) 628-8686
FAX: (602) 244-0446

CALIFORNIA

Intel Corp.
3550 Watt Avenue
Suite 140
Sacramento 95821
Tel: (800) 628-8686
FAX: (916) 488-1473

†Intel Corp.
9665 Chesapeake Dr.
Suite 325
San Diego 92123
Tel: (800) 628-8686
FAX: (619) 292-0628

Intel Corp.
1781 Fox Drive
San Jose 95131
Tel: (800) 628-8686
FAX: (408) 441-9540

*†Intel Corp.
1551 N. Tustin Avenue
Suite 800
Santa Ana 92701
Tel: (800) 628-8686
TWX: 910-595-1114
FAX: (714) 541-9157

†Intel Corp.
15260 Ventura Boulevard
Suite 360
Sherman Oaks 91403
Tel: (800) 628-8686
FAX: (818) 995-6624

COLORADO

*†Intel Corp.
600 S. Cherry St.
Suite 700
Denver 80222
Tel: (800) 628-8686
TWX: 910-931-2289
FAX: (303) 322-8670

CONNECTICUT

†Intel Corp.
103 Mill Plain Road
Danbury 06811
Tel: (800) 628-8686
FAX: (203) 794-0339

FLORIDA

†Intel Corp.
800 Fairway Drive
Suite 160
Deerfield Beach 33441
Tel: (800) 628-8686
FAX: (305) 421-2444

Intel Corp.
2250 Lucien Way
Suite 100-8, 27
Maitland 32751
Tel: (800) 628-8686
FAX: (407) 660-1283

GEORGIA

†Intel Corp.
20 Technology Parkway
Suite 150
Norcross 30092
Tel: (800) 628-8686
FAX: (404) 605-9762

ILLINOIS

*†Intel Corp.
Woodfield Corp. Center III
300 N. Martingale Road
Suite 400
Schaumburg 60173
Tel: (800) 628-8686
FAX: (708) 706-9762

INDIANA

†Intel Corp.
8910 Purdue Road
Suite 350
Indianapolis 46268
Tel: (800) 628-8686
FAX: (317) 875-8938

MARYLAND

*†Intel Corp.
10010 Junction Dr.
Suite 200
Annapolis Junction 20701
Tel: (800) 628-8686
FAX: (410) 206-3678

MASSACHUSETTS

*†Intel Corp.
Westford Corp. Center
5 Carlisle Road
2nd Floor
Westford 01886
Tel: (800) 628-8686
TWX: 710-343-6333
FAX: (508) 692-7867

MICHIGAN

†Intel Corp.
7071 Orchard Lake Road
Suite 100
West Bloomfield 48322
Tel: (800) 628-8686
FAX: (313) 851-8770

MINNESOTA

†Intel Corp.
3500 W. 80th St.
Suite 360
Bloomington 55431
Tel: (800) 628-8686
TWX: 910-576-2867
FAX: (612) 831-6497

NEW JERSEY

*†Intel Corp.
Lincroft Office Center
125 Half Mile Road
Red Bank 07701
Tel: (800) 628-8686
FAX: (908) 747-0983

NEW YORK

*Intel Corp.
850 Crosskeys Office Park
Fairport 14450
Tel: (800) 628-8686
TWX: 510-253-7391
FAX: (716) 223-2561

†Intel Corp.
300 Westage Business Center
Suite 230
Fishkill 12524
Tel: (800) 628-8686
FAX: (914) 897-3125

*†Intel Corp.
2950 Express Dr., South
Suite 130
Islandia 11722
Tel: (800) 628-8686
TWX: 510-227-6236
FAX: (516) 348-7939

OHIO

*Intel Corp.
56 Milford Dr., Suite 205
Hudson 44236
Tel: (800) 628-8686
FAX: (216) 528-1026

*†Intel Corp.
3401 Park Center Drive
Suite 220
Dayton 45414
Tel: (800) 628-8686
TWX: 810-450-2528
FAX: (513) 890-8658

OKLAHOMA

Intel Corp.
6801 N. Broadway
Suite 115
Oklahoma City 73162
Tel: (800) 628-8686
FAX: (405) 840-9819

OREGON

†Intel Corp.
15254 N.W. Greenbrier Pkwy.
Building B
Beaverton 97006
Tel: (800) 628-8686
TWX: 910-467-8741
FAX: (503) 645-8181

PENNSYLVANIA

*†Intel Corp.
925 Harvest Drive
Suite 200
Blue Bell 19422
Tel: (800) 628-8686
FAX: (215) 641-0785

SOUTH CAROLINA

Intel Corp.
7403 Parklane Rd., Suite 3
Columbia 29223
Tel: (800) 628-8686
FAX: (803) 788-7999

Intel Corp.
100 Executive Center Drive
Suite 109, B183
Greenville 29615
Tel: (800) 628-8686
FAX: (803) 297-3401

TEXAS

†Intel Corp.
8911 N. Capital of Texas Hwy.
Suite 4230
Austin 78759
Tel: (800) 628-8686
FAX: (512) 338-9335

*†Intel Corp.
5000 Quorum Drive
Suite 750
Dallas 75240
Tel: (800) 628-8686

*†Intel Corp.
20515 SH 249
Suite 401
Houston 77070
Tel: (800) 628-8686
TWX: 910-881-2490
FAX: (713) 988-3660

UTAH

†Intel Corp.
428 East 6400 South
Suite 135
Murray 84107
Tel: (800) 628-8686
FAX: (801) 268-1457

WASHINGTON

†Intel Corp.
2800 156th Avenue S.E.
Suite 105
Bellevue 98007
Tel: (800) 628-8686
FAX: (206) 746-4495

Intel Corp.
408 N. Mullan Road
Suite 105
Spokane 99206
Tel: (800) 628-8686
FAX: (509) 928-9467

WISCONSIN

Intel Corp.
400 N. Executive Dr.
Suite 401
Brookfield 53005
Tel: (800) 628-8686
FAX: (414) 789-2746

CANADA

BRITISH COLUMBIA

Intel Semiconductor of
Canada, Ltd.
999 Canada Place
Suite 404, #11
Vancouver V6C 3E2
Tel: (800) 628-8686
FAX: (604) 844-2813

ONTARIO

†Intel Semiconductor of
Canada, Ltd.
2650 Queensview Drive
Suite 250
Ottawa K2B 8H6
Tel: (800) 628-8686
FAX: (613) 820-5936

†Intel Semiconductor of
Canada, Ltd.
190 Attwell Drive
Suite 500
Rexdale M9W 6H8
Tel: (800) 628-8686
FAX: (416) 675-2438

QUEBEC

†Intel Semiconductor of
Canada, Ltd.
1 Rue Holiday
Suite 320
Tour East
Pt. Claire H9R 5N3
Tel: (800) 628-8686
FAX: 514-694-0064

†Sales and Service Office
*Field Application Location